

Exhibit-

27F256  
256K (16K x 8) CMOS FLASH MEMORY

- Flash Electrical Chip-Erase
  - 1 Second Typical Chip-Erase *up to 10sec.*
- Quick-Pulse Programming™
  - 100  $\mu$ s Typical Byte-Program
  - 4 Second Chip-Program
- EPROM-Compatible 12.75V  $V_{pp}$  Supply
- 100 Erase/Program Cycles
- High-Performance Speeds
  - 170 ns Maximum Access Time
- Low Power Consumption
  - 100  $\mu$ A Maximum Standby Current
- Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface
- Noise Immunity Features
  - $\pm 10\%$   $V_{CC}$  Tolerance
  - Maximum Latch-Up Immunity through EPI Processing
- ETOX™ Flash-Memory Technology
  - EPROM-Compatible Process Base
  - High-Volume Manufacturing Experience
- Compatible with JEDEC-Standard Byte-Wide EPROM Pinouts
  - 28-Pin "Windowless" Cerdip

(See Packaging Spec., Order # 231369)

Intel's 27F256 CMOS flash-memory offers the most cost-effective and reliable alternative for updatable non-volatile memory. The 27F256 adds electrical chip-erase and reprogramming to familiar EPROM technology. Memory contents can be erased and reprogrammed: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 27F256 increases memory flexibility, while contributing to time- and cost-savings. The 27F256 is targeted for alterable code- or data-storage applications where EPROM ultraviolet erasure is impractical or time consuming. The 27F256 can also be applied where traditional EEPROM functionality (byte-erase) is either not required or not cost-effective.

The 27F256 is a 256-kilobit nonvolatile memory organized as 32768 bytes of 8 bits. Intel's 27F256 is offered in a 28-pin "windowless" cerdip package. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Intel's 27F256 employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 170 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 microamps translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 millamps on address and data pins, from  $-1V$  to  $V_{CC} + 1V$ .

With Intel's ETOX™ (EPROM tunnel oxide) process base, the 27F256 leverages years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. May 1988  
© Intel Corporation, 1988 Order Number: 290157-002

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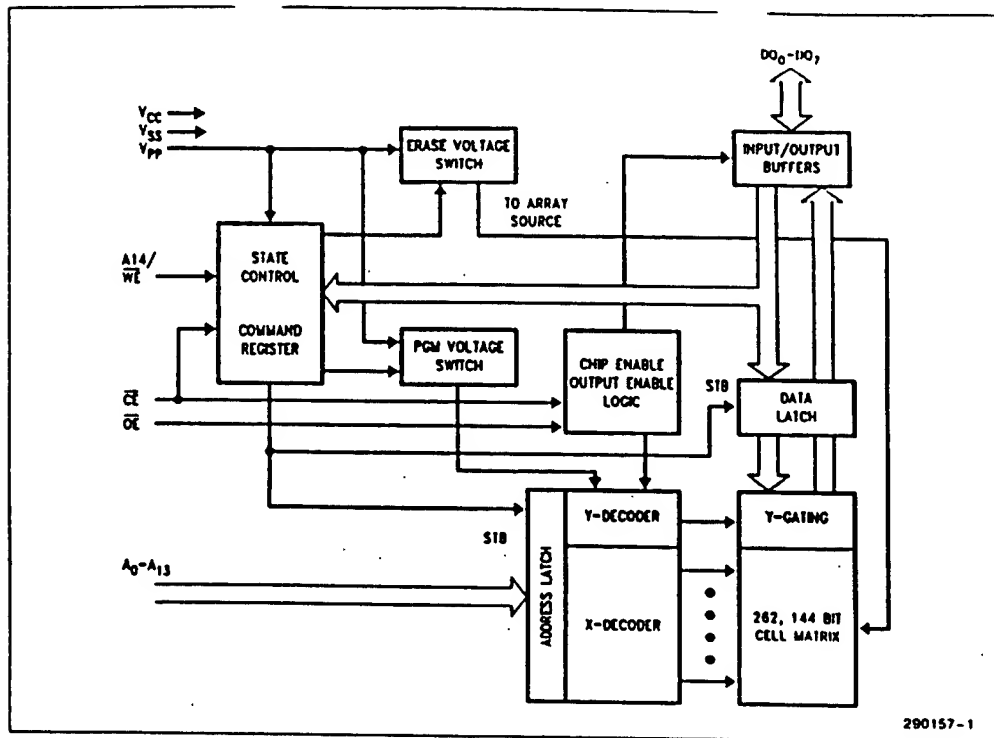


Figure 1. 27F256 Block Diagram

Fl
Syn
$A_0-A$
$DO_0-$
$\overline{CE}$
$\overline{OE}$
$A_{14}/\overline{WE}$
$V_{PP}$
$V_{CC}$
$V_{SS}$

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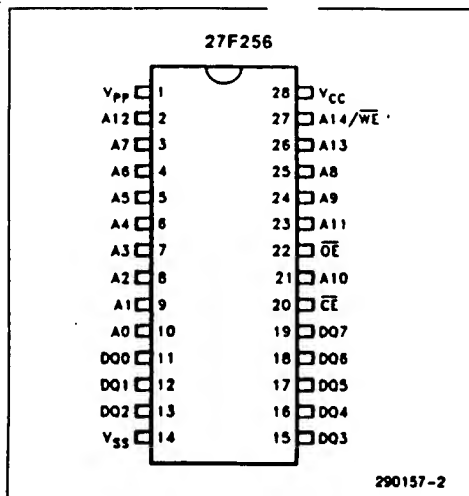


Figure 2. Cerdip (D) Pin Configuration

Table 1. Pin Description

Symbol	Type	Name and Function
A <sub>0</sub> -A <sub>13</sub>	INPUT	<b>ADDRESS INPUTS</b> for memory addresses. Addresses are internally latched during a write cycle.
DQ <sub>0</sub> -DQ <sub>7</sub>	INPUT/ OUTPUT	<b>DATA INPUT/OUTPUT:</b> Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
CE	INPUT	<b>CHIP ENABLE:</b> Activates the device's control logic, input buffers, decoders, and sense amplifiers. CE is active low; CE high deselects the memory device and reduces power consumption to standby levels.
OE	INPUT	<b>OUTPUT ENABLE:</b> Gates the device's output through the data buffers during a read cycle. OE is active low.
A <sub>14</sub> /WE	INPUT	<b>ADDRESS/WRITE ENABLE</b> are multiplexed to maintain EPROM pinout compatibility. With V <sub>pp</sub> high, A <sub>14</sub> /WE functions as the write control pin. With V <sub>pp</sub> low, A <sub>14</sub> /WE functions as an address input line. WE is active low. Addresses are latched on the falling edge of WE. Data is latched on the rising edge of the WE pulse. Note: With V <sub>pp</sub> = V <sub>ppL</sub> , memory contents cannot be altered.
V <sub>pp</sub>		<b>ERASE/PROGRAM POWER SUPPLY</b> for writing the command register, erasing the entire array, or programming bytes in the array.
V <sub>CC</sub>		<b>DEVICE POWER SUPPLY</b> (5V ± 10%)
V <sub>SS</sub>		<b>GROUND</b>

## APPLICATIONS

The 27F256 flash-memory adds electrical chip-erase and reprogrammability to EPROM non-volatility and ease of use. As such, the 27F256 is ideal for storing code or data-tables in embedded control applications where periodic updates are required.

The need for code updates pervades all phases of a system's life—from prototyping to system manufacture to after-sale service. In the factory, during prototyping, revisions to control code necessitate ultraviolet erasure and reprogramming of EPROM-based prototype codes. The 27F256 replaces the 15- to 20-minute ultraviolet erasure with one-second electrical erasure. Electrical chip-erase and reprogramming occur in the same workstation or PROM-programmer socket.

Diagnostics, performed at subassembly or final assembly stages, often require the socketing of EPROMs. Socketed test codes are ultimately replaced with EPROMs containing the final program. With electrical chip-erase and reprogramming, the 27F256 is soldered to the circuit board. Test codes are programmed into the 27F256 as it resides on the circuit board. Ultimately, the final code can be downloaded to the device. The 27F256's in-circuit alterability eliminates unnecessary handling and less-reliable socketed connections, while adding greater test flexibility.

Material and labor costs associated with code changes increase at higher levels of system integration—the most costly being code updates after sale. Code "bugs", or the desire to augment system func-

tionality, prompt after-sale code updates. Field revisions to EPROM-based code require the removal of EPROM components or entire boards. The service technician performs the twenty-minute ultraviolet erasure and reprogramming on-site, or returns boards to the factory for rework. An alternate approach is to use one-time-programmable EPROMs. The service technician removes the "old" devices and replaces them with updated versions. The used components are discarded.

Designing with the in-circuit alterable 27F256 eliminates socketed memories, reduces overall material costs, and drastically cuts the labor costs associated with code updates. With the 27F256, code updates are implemented locally via an edge-connector, or remotely over a serial communication link.

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 3 illustrates the interface between the MCS-51 microcontroller and one 27F256 flash-memory in a minimum chip-count system. Figure 4 depicts two 27F256s tied to the 80C186 system bus. In both instances, the 27F256's architecture minimizes interface circuitry needed for complete in-circuit updates of memory contents.

With cost-effective electrical erasure and reprogramming, the 27F256 fills the functionality gap between traditional EPROMs and EEPROMs. EEPROM-compatible specifications, straightforward interfacing, and in-circuit alterability allows designers to easily augment memory flexibility and satisfy the need for updatable-code-storage in today's designs.

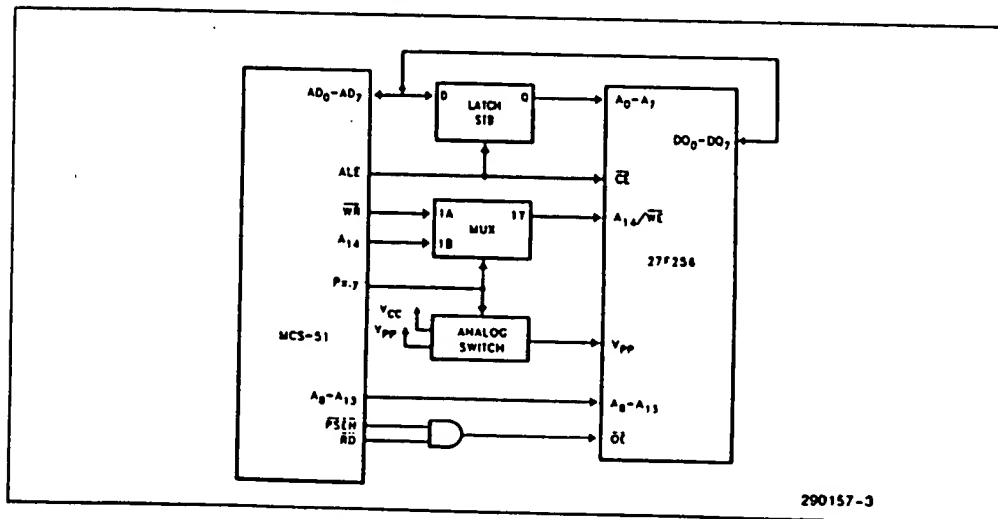


Figure 3. 27F256 in an MCS-51 System

80C1  
SYSTEM

A1-1

DO0-D7

DO0-1

MC

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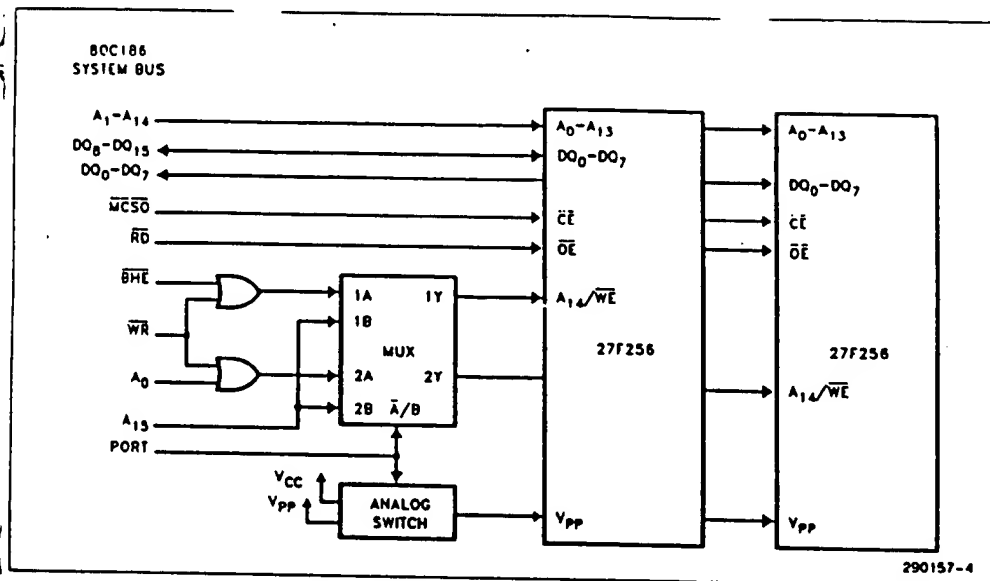
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## PRINCIPLE

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## PRINCIPLES OF OPERATION

In the absence of high voltage on the V<sub>pp</sub> pin, the 27F256 is a read-only memory. The 27F256 is completely read-compatible with the industry-standard 27256 and 27C256 EPROMs. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and intelligent Identifier™ operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the Vpp pin. In addition, high voltage on Vpp enables erasure and programming of the device. All functions associated with altering memory contents—Intelligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the intelligent Identifier codes, or output data for erase and program verification.

Table 2. 27F256 Bus Operations

Pins		V <sub>PP</sub> (1)	A <sub>0</sub>	A <sub>9</sub>	CE	OE	A14/ WE	DO <sub>0</sub> -DO <sub>7</sub>
READ-ONLY	Read	V <sub>PPL</sub>	A <sub>0</sub>	A <sub>9</sub>	V <sub>IL</sub>	V <sub>IL</sub>	A <sub>14</sub>	Data Out
	Output Disable	V <sub>PPL</sub>	X	X	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Tri-state
	Standby	V <sub>PPL</sub>	X	X	V <sub>IH</sub>	X	X	Tri-state
	Intelligent ID™ Manufacturer (2)	V <sub>PPL</sub>	V <sub>IL</sub>	V <sub>ID</sub> (3)	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	Data = 89H
	Intelligent ID™ Device (2)	V <sub>PPL</sub>	V <sub>IH</sub>	V <sub>ID</sub> (3)	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	Data = 91H
READ/ WRITE	Read	V <sub>PPH</sub>	A <sub>0</sub>	A <sub>9</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Data Out (4)
	Output Disable	V <sub>PPH</sub>	X	X	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Tri-state
	Standby (5)	V <sub>PPH</sub>	X	X	V <sub>IH</sub>	X	X	Tri-state
	Write	V <sub>PPH</sub>	A <sub>0</sub>	A <sub>9</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Data In (6)

## NOTES:

1. V<sub>PPL</sub> may be ground, a no-connect with a resistor tied to ground, or  $\leq V_{CC} + 2.0V$ . V<sub>PPH</sub> is the programming voltage specified for the device. Refer to D.C. Characteristics. When V<sub>PP</sub> = V<sub>PPL</sub>, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3.
3.  $11.5V \leq V_{ID} \leq 13.0V$ .
4. Read operations with V<sub>PP</sub> = V<sub>PPH</sub> may access array data or the Intelligent ID™.
5. With V<sub>PP</sub> at high voltage, the standby current equals I<sub>CC</sub> + I<sub>PP</sub> (standby).
6. Refer to Table 3 for valid Data-In during a write operation.
7. X can be V<sub>IL</sub> or V<sub>IH</sub>.

The command register is only alterable when V<sub>PP</sub> is at high voltage. Depending upon the application, the system designer may choose to make the V<sub>PP</sub> power supply switchable—available only when memory updates are desired. When high voltage is removed, the contents of the register default to the read command, making the 27F256 a read-only memory. Memory contents cannot be altered.

Write-Enable control is multiplexed with A14 to preserve compatibility with EPROM footprints. When V<sub>PP</sub> equals V<sub>PPH</sub>, A14/Write-Enable functions as the Write-Enable pin. When V<sub>PP</sub> equals V<sub>PPL</sub>, A14/Write-Enable is an address input line. The lowest order register bit contains the A14 information. In this manner, the 27F256 operates in a page-addressed fashion when V<sub>PP</sub> equals V<sub>PPH</sub>.

The system designer may choose to "hard-wire" V<sub>PP</sub>, making the high voltage supply constantly available. In this instance, all operations are performed in conjunction with the command register. The 27F256 is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

## BUS OPERATIONS

## Read

The 27F256 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable (CE) is the power control and should be used for device selection. Output-Enable (OE) is the output control and should be used to gate data from the output pins, independent of device selection. Figure 7 illustrates read timing waveforms.

The read operation only accesses array data when V<sub>PP</sub> is low (V<sub>PPL</sub>). When V<sub>PP</sub> is high (V<sub>PPH</sub>), the read operation can be used to access array data, to output the Intelligent Identifier™ codes, and to access data for program/erase verification.

## Output Disable

With Output-Enable at a logic-high level (V<sub>IH</sub>), output from the device is disabled. Output pins are placed in a high-impedance state.

## Standby

With Chip-Enable (CE) at a logic-high level, the 27F256 enters a standby mode. The output pins are in a high-impedance state, independent of the state of the output pins. The 27F256 draws no current from the system.

## Intelligent ID

The Intelligent ID™ is a unique code assigned to each device. It is used for device identification and is stored in the command register.

With Chip-Enable (CE) at a logic-high level, the 27F256 enters a standby mode. The output pins are in a high-impedance state, independent of the state of the output pins. The 27F256 draws no current from the system.

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## Write

Device erasure is accomplished by the command register. The command register is used to store data information. The command register is used to store data information. The command register is used to store data information.

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Q0-DQ7

Data Out

tri-state

tri-state

A = 89H

A = 91H

Data Out (4)

tri-state

tri-state

Data In (8)

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## Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the 27F256's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the Output-Enable signal. If the 27F256 is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

## Intelligent Identifier™

The Intelligent Identifier operation outputs the manufacturer code (89H) and device code (91H). Programming equipment automatically matches the device with its proper erase and programming algorithms.

With Chip-Enable and Output-Enable at a logic low level, raising A9 to high voltage (11.5V–13.0V) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the 27F256 is erased and reprogrammed in the target system. Following a write of 80H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (91H).

## Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the Vpp pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing Write-Enable to logic-low level (V<sub>IL</sub>), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

The three high-order register bits (R7, R6, R5) encode the control functions. The lowest-order register bit (R0) contains the A14 information. All other regis-

ter bits, R4 to R1, must be zero. The only exception is the reset command, when FFH is written to the register. Register bits R7–R0 correspond to data inputs D7–D0.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

## COMMAND DEFINITIONS

When low voltage is applied to the Vpp pin, the contents of the command register default to 00H, enabling read-only operations. Placing high voltage on the Vpp pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these 27F256 register commands.

### Read Command (Page 0/Page 1)

While Vpp is high, for erasure and programming, memory contents can be accessed via the read command. When accessing array data with the read command, the A14 address information is written into bit zero (R0) of the command register. In effect, this divides the device into 16-kilobyte pages (page 0 and page 1).

The read operation (page 0) is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data from the lower 16-kilobyte page of memory. The device remains enabled for reads (page 0) until the command register contents are altered. By writing 01H to the command register, read cycles access data from the upper 16-kilobyte page (page 1) of memory.

The default contents of the register upon Vpp power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the Vpp power transition. Where the Vpp supply is hard-wired to the 27F256, the device powers-up and remains enabled for reads (page 0) until the command-register contents are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

### Intelligent Identifier™ Command

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not desired system-design practice.

Table 3. Command Definitions

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory							
a. Page 0	1	Write	X	00H			
b. Page 1	1	Write	X	01H			
Read Intelligent ID™	1	Write	X	80H			
Set-up Erase/Eraser(4)	2	Write	X	20H	Write	X	20H
Erase Verify(4)							
a. Page 0	2	Write	EA	A0H	Read	X	EVD
b. Page 1	2	Write	EA	A1H	Read	X	EVD
Set-up Program/Program(5)							
a. Page 0	2	Write	X	40H	Write	PA	PD
b. Page 1	2	Write	X	41H	Write	PA	PD
Program Verify(5)							
a. Page 0	2	Write	X	C0H	Read	X	PVD
b. Page 1	2	Write	X	C1H	Read	X	PVD
Reset(6)	2	Write	X	FFH	Write	X	FFH

NOTES:

1. Bus operations are defined in Table 2.
2. EA = Address of memory location to be read during erase verify.  
PA = Address of memory location to be programmed.  
Addresses are latched on the falling edge of the Write-Enable pulse.
3. EVD = Data read from location EA during erase verify.  
PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.  
PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Figure 6 illustrates the Quick-Erase™ Algorithm.
5. Figure 5 illustrates the Quick-Pulse Programming™ Algorithm.
6. The second bus cycle must be followed by the desired command register write.

The 27F256 contains an intelligent Identifier™ operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 80H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of 91H. To terminate the operation, it is necessary to write another valid command into the register.

### Set-up Erase/Eraser Commands

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e. Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V<sub>PP</sub> pin. In the absence of this high voltage, memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

### Erase-Verify Command (Page 0/Page 1)

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must

be verified, initiated by writing FFH to the register. The verify command must be supplied to the Write-Enable pulse to ensure the erase operation is successful.

The 27F256 voltage to the array is erased.

The erase-verify command relatches its address byte in the return FFH is acknowledged, must be within boundary.

In the case of erase operation, the address of the array has to be programmed. The verify command relatches its address byte in the return FFH is acknowledged, must be within boundary.

### Set-up Program (Page 0/F

Set-up program stages the device for programming of the array (page 0) or performs the register to set.

Once the device is in the active program mode, the next Write-Enable pulse will latch the address byte of the Write-Enable pulse. The program operation is performed by writing the program data to the array. The program operation is performed by writing the program data to the array. The program operation is performed by writing the program data to the array.



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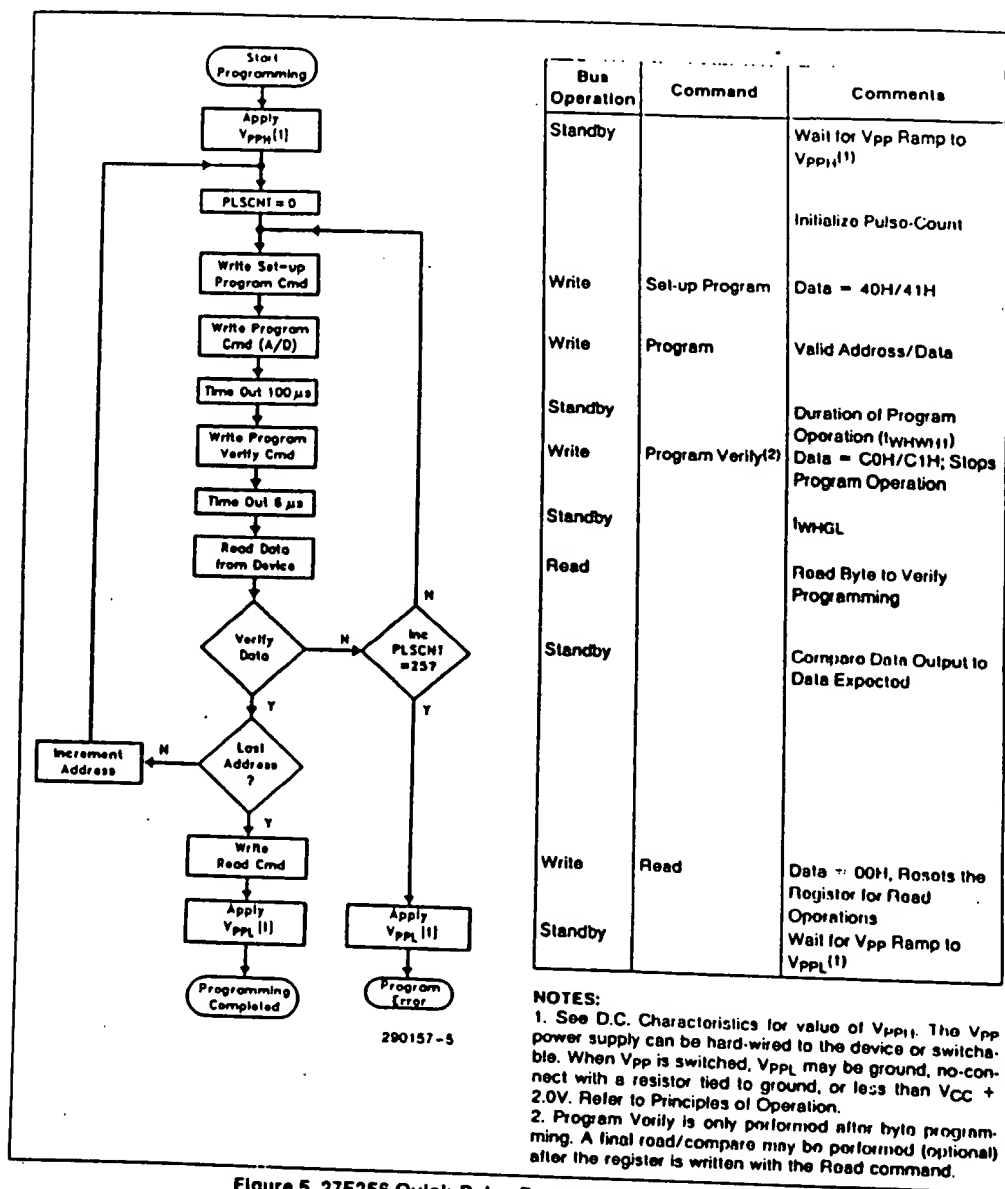


Figure 5. 27F256 Quick-Pulse Programming™ Algorithm

## QUICK-ERASE™ ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming™ algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The 27F256 is erased when shipped from the factory, loading FFH data from the device would immediately be followed by device programming.

Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately four seconds.

Erasure execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. A total of sixty-four erase operations are allowed, which corresponds to approximately ten seconds of cumulative erase time. Erasure typically occurs in one second. Figure 6 illustrates the Quick-Erase Algorithm.

## DESIGN CONSIDERATIONS

### Two-Line Output Control

Flash memories are often used in larger memory arrays. Intel provides two read-control inputs to accommodate multiple memory connections. Two-line control provides for:

- a) the lowest possible memory power dissipation, and
- b) complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address-decoder output should drive chip-enable, while the system's read signal controls all flash memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

### Power Supply Decoupling

Flash-memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I<sub>CC</sub>) issues—standby, active and transient current peaks produced by falling and rising edges of Chip-Enable. The capacitive and inductive loads on the device outputs determine the magnitudes of those peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1  $\mu$ F ceramic capacitor connected between V<sub>CC</sub> and V<sub>SS</sub>, and between V<sub>PP</sub> and V<sub>SS</sub>.

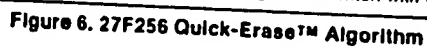
Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7  $\mu$ F electrolytic capacitor should be placed at the array's power supply connection, between V<sub>CC</sub> and V<sub>SS</sub>. The bulk capacitor will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

### V<sub>PP</sub> Trace on Printed Circuit Boards

Programming flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V<sub>PP</sub> power supply trace. The V<sub>PP</sub> pin supplies the memory cell current for programming. Use similar trace width and layout considerations given the V<sub>CC</sub> power bus. Adequate V<sub>PP</sub> supply traces and decoupling will decrease V<sub>PP</sub> voltage spikes and overshoots.

### Power Up/Down Sequencing

The 27F256 is designed to offer protection against accidental erasure or programming, caused by spurious system-level signals that may exist during power transitions. The 27F256 powers-up in its read-only state. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of the two-step command sequences. While these precautions are sufficient for most applications, it is recommended that V<sub>CC</sub> reach its steady-state value before raising V<sub>PP</sub> above V<sub>CC</sub> + 2.0V. In addition, upon powering-down, V<sub>PP</sub> should be below V<sub>CC</sub> + 2.0V, before lowering V<sub>CC</sub>.



**NOTES:**

1. See D.C. Characteristics for value of  $V_{PP1}$ . The  $V_{PP}$  power supply can be hard-wired to the device or switchable. When  $V_{PP}$  is switched,  $V_{PP1}$  may be ground, no-connect with a resistor tied to ground, or less than  $V_{CC} + 2.0V$ . Refer to Principles of Operation.
2. Erase Verily is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.

**NOTES:**  
Operating temperature  
Minimum D.C. input voltage  
Maximum D.C. voltage  
Maximum D.C. voltage  
Output shorted for no

Symbol	
I <sub>LI</sub>	Input
I <sub>LO</sub>	Output
I <sub>CCS</sub>	V <sub>CC</sub>
I <sub>CC1</sub>	V <sub>CC</sub>
I <sub>CC2</sub>	V <sub>CC</sub>

## ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0°C to +70°C <sup>(1)</sup>
During Read	0°C to +70°C
During Erase/Program	0°C to +70°C
Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V <sup>(2)</sup>
Voltage on Pin A <sub>0</sub> with Respect to Ground	-2.0V to +13.5V <sup>(2,3)</sup>
V <sub>pp</sub> Supply Voltage with Respect to Ground	
During Erase/Program	-2.0V to +14.0V <sup>(2,3)</sup>
V <sub>cc</sub> Supply Voltage with Respect to Ground	-2.0V to +7.0V <sup>(2)</sup>
Output Short Circuit Current	100 mA <sup>(4)</sup>

*\*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**NOTICE:** Specifications contained within the following tables are subject to change.

### NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum D.C. input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods less than 20ns.
3. Maximum D.C. voltage on output pins is V<sub>CC</sub> + 0.5V, which may overshoot to V<sub>CC</sub> + 2.0V for periods less than 20ns.
4. Maximum D.C. voltage on A<sub>0</sub> or V<sub>pp</sub> may overshoot to +14.0V for periods less than 20 ns.

Output shorted for no more than one second. No more than one output shorted at a time.

## OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T <sub>A</sub>	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage	4.50	5.50	V	

## D.C. CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I <sub>I</sub>	Input Leakage Current		± 1.0	μA	V <sub>CC</sub> = V <sub>CC</sub> max V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub>
I <sub>O</sub>	Output Leakage Current		± 1.0	μA	V <sub>CC</sub> = V <sub>CC</sub> max V <sub>OUT</sub> = V <sub>CC</sub> or V <sub>SS</sub>
I <sub>CCS</sub>	V <sub>CC</sub> Standby Current		1.0	mA	V <sub>CC</sub> = V <sub>CC</sub> max CE = V <sub>IL</sub>
I <sub>CC1</sub>	V <sub>CC</sub> Active Read Current		30	mA	V <sub>CC</sub> = V <sub>CC</sub> max CE = V <sub>IL</sub> f = 6MHz, I <sub>OUT</sub> = 0 mA
I <sub>CC2</sub>	V <sub>CC</sub> Programming Current		30	mA	CE = V <sub>IL</sub> Programming in progress

D.C. CHARACTERISTICS—TTL/NMOS COMPATIBLE (Continued)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
$I_{CC3}$	$V_{CC}$ Erase Current		30	mA	$\overline{CE} = V_{IL}$ Erase in progress
$I_{PP5}$	$V_{pp}$ Standby Current		1.0	$\mu A$	$V_{PP} = V_{PPL}$
$I_{PP1}$	$V_{pp}$ Read Current		200	$\mu A$	$V_{PP} = V_{PPH}$
$I_{PP2}$	$V_{pp}$ Programming Current		30	mA	$V_{PP} = V_{PPH}$ Programming in progress
$I_{PP3}$	$V_{pp}$ Erase Current		30	mA	$V_{PP} = V_{PPH}$ Erase in progress
$V_{IL}$	Input Low Voltage	-0.5	0.8	V	
$V_{IH}$	Input High Voltage	2.0	$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage		0.45	V	$I_{OL} = 2.1 \text{ mA}$ $V_{CC} = V_{CC \text{ min}}$
$V_{OH1}$	Output High Voltage	2.4		V	$I_{OH} = -2.5 \text{ mA}$ $V_{CC} = V_{CC \text{ min}}$
$V_{ID}$	$A_9$ Intelligent Identifier™ Voltage	11.50	13.00	V	$A_9 = V_{ID}$
$I_{ID}$	$A_9$ Intelligent Identifier™ Current		500	$\mu A$	$A_9 = V_{ID}$
$V_{PPL}$	$V_{pp}$ during Read-Only Operations	0.00	$V_{CC} + 2.0V$	V	Note: Erase/Program are inhibited when $V_{PP} = V_{PPL}$
$V_{PPH}$	$V_{pp}$ during Read/Write Operations	12.50	13.00	V	

D.C. CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
$I_{LI}$	Input Leakage Current		$\pm 1.0$	$\mu A$	$V_{CC} = V_{CC \text{ max}}$ $V_{IN} = V_{CC} \text{ or } V_{SS}$
$I_{LO}$	Output Leakage Current		$\pm 1.0$	$\mu A$	$V_{CC} = V_{CC \text{ max}}$ $V_{OUT} = V_{CC} \text{ or } V_{SS}$
$I_{CCS}$	$V_{CC}$ Standby Current		100	$\mu A$	$V_{CC} = V_{CC \text{ max}}$ $\overline{CE} = V_{IH}$

D.C. CHARAC

Symbol	
$I_{CC1}$	$V_{CC} A$
$I_{CC2}$	$V_{CC} P$
$I_{CC3}$	$V_{CC} E$
$I_{PP5}$	$V_{PP} S$
$I_{PP1}$	$V_{PP} R$
$I_{PP2}$	$V_{PP} P$
$I_{PP3}$	$V_{PP} E$
$V_{IL}$	Input L
$V_{IH}$	Input H
$V_{OL}$	Output
$V_{OH1}$	Output
$V_{OH2}$	
$V_{ID}$	$A_9$ inte Voltage
$I_{ID}$	$A_9$ inte Current
$V_{PPL}$	$V_{PP}$ dur Operati
$V_{PPH}$	$V_{PP}$ dur Operati

APACITANCE(1)

Symbol	
$C_{IN}$	
$C_{OUT}$	

NOTE: Sampled, not 100%

## D.C. CHARACTERISTICS—CMOS COMPATIBLE (Continued)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
$I_{CC1}$	$V_{CC}$ Active Read Current		20	mA	$V_{CC} = V_{CC \text{ max}}$ $\overline{CE} = V_{IL}$ $f = 6\text{ MHz}$ , $I_{OUT} = 0\text{ mA}$
$I_{CC2}$	$V_{CC}$ Programming Current		30	mA	$\overline{CE} = V_{IH}$ Programming in progress
$I_{CC3}$	$V_{CC}$ Erase Current		30	mA	$\overline{CE} = V_{IL}$ Erase in progress
$I_{PPS}$	$V_{PP}$ Standby Current		1.0	$\mu\text{A}$	$V_{PP} = V_{PPL}$
$I_{PP1}$	$V_{PP}$ Read Current		200	$\mu\text{A}$	$V_{PP} = V_{PPH}$
$I_{PP2}$	$V_{PP}$ Programming Current		30	mA	$V_{PP} = V_{PPH}$ Programming in progress
$I_{PP3}$	$V_{PP}$ Erase Current		30	mA	$V_{PP} = V_{PPH}$ Erase in progress
$V_{IL}$	Input Low Voltage	-0.5	0.8	V	
$V_{IH}$	Input High Voltage	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage		0.45	V	$I_{OL} = 2.1\text{ mA}$ $V_{CC} = V_{CC \text{ min}}$
$V_{OH1}$	Output High Voltage	$0.85 V_{CC}$		V	$I_{OH} = -2.5\text{ mA}$ $V_{CC} = V_{CC \text{ min}}$
$V_{OH2}$		$V_{CC} - 0.4$			$I_{OH} = -100\text{ }\mu\text{A}$ $V_{CC} = V_{CC \text{ min}}$
$V_{ID}$	$A_9$ Intelligent Identifier™ Voltage	11.50	13.00	V	$A_9 = V_{ID}$
$I_{ID}$	$A_9$ Intelligent Identifier™ Current		500	$\mu\text{A}$	$A_9 = V_{ID}$
$V_{PPL}$	$V_{PP}$ during Read-Only Operations	0.00	$V_{CC} + 2.0$	V	Note: Erase/Program are inhibited when $V_{PP} = V_{PPL}$
$V_{PPH}$	$V_{PP}$ during Read/Write Operations	12.50	13.00	V	

CAPACITANCE(1)  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ 

Symbol	Parameter	Limits		Unit	Conditions
		Min	Max		
$C_{IN}$	Address/Control Capacitance		6	pF	$V_{IN} = 0\text{ V}$
$C_{OUT}$	Output Capacitance		12	pF	$V_{OUT} = 0\text{ V}$

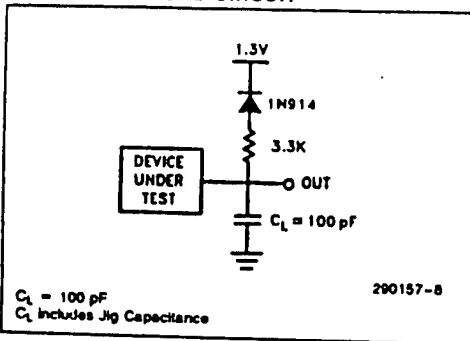
## NOTE:

1. Sampled, not 100% tested.

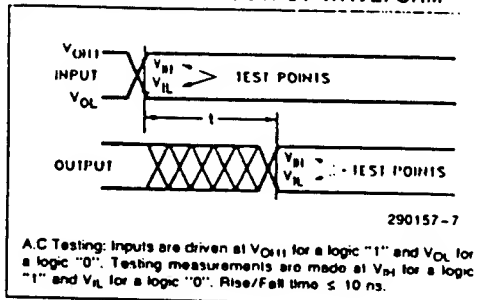
### A.C. TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) ..... 10 ns  
 Input Pulse Levels .....  $V_{OL}$  and  $V_{OH}$   
 Input Timing Reference Level .....  $V_{IL}$  and  $V_{IH}$   
 Output Timing Reference Level .....  $V_{OL}$  and  $V_{OH}$

### A.C. TESTING LOAD CIRCUIT



### A.C. TESTING INPUT/OUTPUT WAVEFORM



### A.C. CHARACTERISTICS—READ-ONLY OPERATIONS

Versions		27F256-170P2C2		27F256-200P2C2		27F256-250P2C2		Unit
Symbol	Characteristics	Min	Max	Min	Max	Min	Max	
$t_{AVAV}/t_{RC}$	Read Cycle Time	170		200		250		ns
$t_{ELOV}/t_{CE}$	Chip Enable Access Time		170		200		250	ns
$t_{AVOV}/t_{ACC}$	Address Access Time		170		200		250	ns
$t_{GLOV}/t_{OE}$	Output Enable Access Time		70		75		80	ns
$t_{ELOX}/t_{LZ}$	Chip Enable to Output in Low Z	0		0		0		ns
$t_{EHQZ}$	Chip Enable to Output in High Z		55		60		65	ns
$t_{GLOX}/t_{OLZ}$	Output Enable to Output in Low Z	0		0		0		ns
$t_{GHOZ}/t_{DF}$	Output Disable to Output in High Z		35		45		55	ns
$t_{OH}$	Output Hold from Address, CE, or OE Change (1)	0		0		0		ns
$t_{WHGL}$	Write Recovery Time Before Read	6		6		6		ns

NOTES:  
 1. Whichever occurs first.  
 2. Rise/Fall times  $\leq 10$  ns.





**Figure 7. AC Waveforms for Read Operations**

**SAN002157**

## A.C. CHARACTERISTICS—For Write/Erase/Program Operations(1)

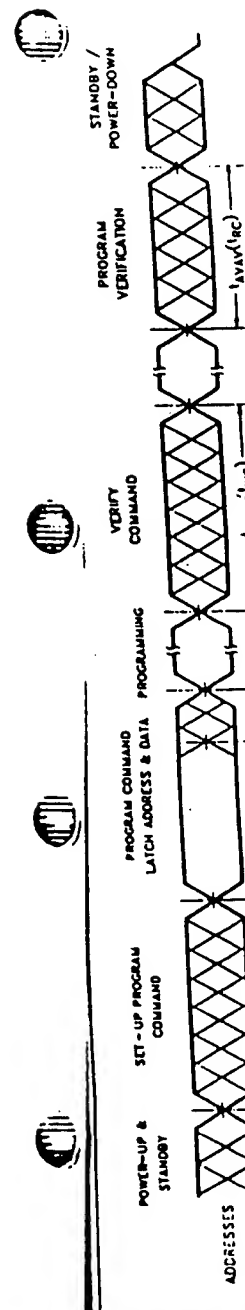
Versions		27F256-170P2C2		27F256-200P2C2		27F256-250P2C2		Unit
Symbol	Characteristics	Min	Max	Min	Max	Min	Max	
t <sub>AVAV</sub> /t <sub>WC</sub>	Write Cycle Time	170		200		250		ns
t <sub>AVWL</sub> /t <sub>AS</sub>	Address Set-up Time	0		0		0		ns
t <sub>WLAX</sub> /t <sub>AH</sub>	Address Hold Time	60		75		90		ns
t <sub>DVWH</sub> /t <sub>DS</sub>	Data Set-up Time	50		50		50		ns
t <sub>WHDX</sub> /t <sub>DH</sub>	Data Hold Time	10		10		10		ns
t <sub>WHGL</sub>	Write Recovery Time Before Read	6		6		6		μs
t <sub>GHWL</sub>	Read Recovery Time Before Write	0		0		0		μs
t <sub>ELWL</sub> /t <sub>CS</sub>	Chip Enable Set-up Time	0		0		0		ns
t <sub>WEH</sub> /t <sub>CH</sub>	Chip Enable Hold Time	0		0		0		ns
t <sub>WLWH</sub> /t <sub>WP</sub>	Write Pulse Width	50		60		75		ns
t <sub>WHWL</sub> /t <sub>WPH</sub>	Write Pulse Width High	50		60		75		ns
t <sub>WHWH1</sub>	Programming Operation	95	150	95	150	95	150	μs
t <sub>WHWH2</sub>	Erase Operation	(2)	(2) + 5%	(2)	(2) + 5%	(2)	(2) + 5%	
t <sub>EHVP</sub>	Chip Enable Set-up Time to V <sub>pp</sub> Ramp	100		100		100		ns
t <sub>VPEL</sub>	V <sub>pp</sub> Set-up Time to Chip Enable Low	100		100		100		ns

## NOTES:

- Read timing characteristics during read/write operations are the same as during read-only operations. Refer to A.C. Characteristics for Read-Only Operations.
- The duration of each erase operation is variable and is calculated in the Quick-Erase™ Algorithm. The duration of the current erase operation is equal to the truncated value of cumulative erase time divided by eight (integer divide).

$$TEW = \text{Integer Divide (CUMTEW/8)}$$

The duration of the erase operation actually applied can exceed the calculated value by a maximum tolerance of 5%. Refer to Figure 6 for additional details.

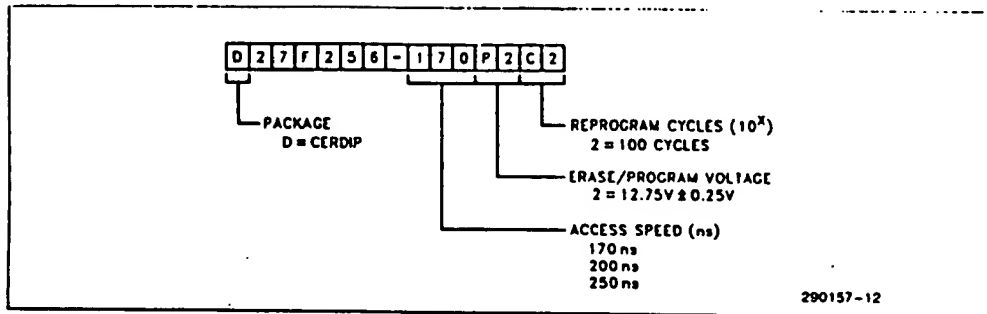




**SAN002159**



ORDERING INFORMATION



VALID COMBINATIONS:

D27F256-170P2C2

D27F256-200P2C2

D27F256-250P2C2